Imperial College London
Department of Electrical & Electronic Engineering

E2 Circuits & Systems – End-of-term Lab Oral 2025 (updated)

The Final Lab Oral will be in the form of a 15 minutes individual oral examination conducted in person in the Lab. This will take place on Tuesday 9th or Wednesday 10th of December 2025. The purpose of this end-of-term lab oral is to assess your level of attainment in the intended learning outcomes for Lab 3 to Lab 6, and to give you a chance to "show off" your achievement and understanding with the Challenge(s). A schedule for the oral examination is attached. **This is a formal assessment.** If you wish to swap your time slot with someone else, you must find a willing person to swap with, and let me know in advance via email, and no later than Monday 8th of December.

Logbook

You must have your electronics logbook with you at the Oral Examination ready to show to your examiner. Although your logbook will NOT be "marked" in the conventional sense, your examiner will nevertheless judge how much you have engaged and achieved in these second half of the term. You will also be asked questions that can **only** be answered by referring to the logbook.

Challenges

If you managed to complete one or more of the Challenges, you must **take a video** of your achievements and share this with your Assessor. DO NOT PERFORM DEMONSTRATION LIVE. There is not enough time, and it may go wrong on the day.

Format of the Oral – You must arrive in the Level 1 Lab at least 5 minutes before your allocated time. Your Examiner will invite you to join when he/she is ready. You will be asked questions on Lab 3 to Lab 6. These questions are designed to determine how much you understand the principles behind the experiments, how much you have engaged, and how much you have learned. You will also be asked to show demo on any challenges you may have completed. You may also be asked questions about the challenges to make sure that you did them and understand what you have done

Grading – Attached is the marksheet that your Examiner will be using during the oral examination. You will be given two grades: one for Lab 3 to 6 (15%), and one for the challenges (10%). The assessment form with feedback will be returned to you via email just before start of next term. Your will receive a grade for the Labs according to the criteria shown below:

A = Excellent (70%+)	Completed all, and understood everything with no gap in knowledge
B = Good (60%+)	Completed all or nearly all, with good understanding but with minor gaps
C = OK (50%+)	Fair understanding with some gaps, completed most parts
D = Weak (40%+)	Weak understanding with many gaps
E = Fail (below 40%).	Very weak understanding, lack evidence of real effort

The Challenges are designed at different levels. The grade range for the level attained are:

Highest Level completed	Grade range
Level 1: Random noise generator	C+ to C-
Level 2: Real-time clock/Basic variable sine gen	B- to B
Level 3: Sine gen with stretched goal	A- to A
Level 4: F1 light control/variable delay echo	A+ to A-

We expect the average mark for this assessment to be around 62 to 68% for the entire class. To ensure fair assessment, I will perform moderation of marks between different Examiners and apply adjustments as I see fit.

Lab-in-a-Box RETURN

You must return the Lab-in-a-Box to one of the technicians in the Level 1 Lab AND the DE10-Lite FPGA board to the stores. You final Lab Oral marksheet will only be released to you at the start of the term and AFTER you have returned the Box unless you have informed me via email that you wish to keep the equipment over the holiday.

Learning Outcomes

Lab 3 & 4 – Counters and Shift Registers

- Explain the workflow in turning a design in SystemVerilog to FPGA bit-stream
- Explain how a basic counter is specified in SystemVerilog
- Explain the link between SystemVerilog and the actual hardware produced (RTL viewer)
- Explain the propagation delay information as reported by Timing Analyzer
- Explain the working of a shift register, LFSR and PRBS
- Explain the concept of using single clock with enable signal
- Explain the binary to BCD conversion algorithm and its use

Lab 5 – DAC and Function Generator

- Explain PWM with LPF as digital to analogue conversion
- Explain limitations and benefits of PWM as a method of DAC
- Explain the working of the DAC chip used in experiment and its specifications
- Explain SPI interface signals
- Explain how to combine counters and other circuits to provide a variable frequency function generator

Lab 6 – ADC and Echo Synthesizer

- Explain the signal flow in the analogue-digital combined system
- Explain why remove of offset to converted digital signal is required
- Explain the "***allpass***" processor module in the context of the basic system
- Explain how the "***single echo***" design works
- Explain how the multiple echo design works

You are expected to complete at least one of the Challenges. The highest level of difficulty of the Challenges you have completed is linked to the Challenge grade according to the table shown above.

Peter Cheung
Version 3.1, 2 December 2025.

Imperial College London

Department of Electrical & Electronic Engineering

EE2 Circuits and Systems Module
End-of-term Lab Oral

Name of Student:

Names of Assessors:

Date: Tue/Wed

Performance on the Lab 3 to 6 **Experimen Grade (15%):**

1. Logbook Quality and Effectiveness

Highly effective | Effective | OK | Weak | Poor

2. Ability to answer questions from the logbook

Excellent | Good | OK | Poor | Very poor

3. Effort to completing Lab 3 to 6

Fully engaged Strong evidence | Good engagement Good evidence | Acceptable Engagement | Below expected Engagement | V. poor Engagement

4. Understanding of the experiments

Excellent | Good | OK | Poor | Very poor

Performance on the Challengeas

5. Challenge Attempt or Completed

Challenge completed (say which) | Challenge attempted | Did not attempt

6. Examiner's opinion on candidate's depth of understanding in general

Broad & deep | Good | Average | Less than average | Poor

FEEDBACK TO STUDENT: **Challenge GRAD (10%):**

ELEC50001 Circuits and Systems - End-of-Term Lab Oral 9-10 December 2025

First name	Last name	Date	Time	Examiner
Ava	Amar	Tue 9th	09.00 - 09.15	Assessor 1
Alexandros	Psyllidis	Tue 9th	09.00 - 09.15	Assessor 2
Edward	Sandeman	Tue 9th	09.00 - 09.15	Assessor 3
Yida	Wu	Tue 9th	09.00 - 09.15	Assessor 4
Eugene	Gardiner	Tue 9th	09.15 - 09.30	Assessor 1
Vo	Tran	Tue 9th	09.15 - 09.30	Assessor 2
Rohan	Kapisthalam	Tue 9th	09.15 - 09.30	Assessor 3
Eden	Wong	Tue 9th	09.15 - 09.30	Assessor 4
Wei	Tan	Tue 9th	09.30 - 09.45	Assessor 1
Ryan	Parsons	Tue 9th	09.30 - 09.45	Assessor 2
Herbie	Skidmore	Tue 9th	09.30 - 09.45	Assessor 3
Hemapriya	Karthikeyan	Tue 9th	09.30 - 09.45	Assessor 4
Samuel	Snelson-Wash	Tue 9th	09.45 - 10.00	Assessor 1
Ziyi	Liu	Tue 9th	09.45 - 10.00	Assessor 2
Niklas	Tikka	Tue 9th	09.45 - 10.00	Assessor 3
Archie	Eltherington	Tue 9th	09.45 - 10.00	Assessor 4
Phuong	Vo	Tue 9th	10.00 - 10.15	Assessor 1
Zhiyuan	Shi	Tue 9th	10.00 - 10.15	Assessor 2
Yuhan	Zou	Tue 9th	10.00 - 10.15	Assessor 3
Hoi	Chou	Tue 9th	10.00 - 10.15	Assessor 4
Zeb	Forde-Smith	Tue 9th	10.15 - 10.30	Assessor 1
Peixin	Yao	Tue 9th	10.15 - 10.30	Assessor 2
Ian	Leary	Tue 9th	10.15 - 10.30	Assessor 3
Tin	Maicharoensre	Tue 9th	10.15 - 10.30	Assessor 4
Clementine	White	Tue 9th	10.30 - 10.45	Assessor 1
KRISH	KOTHARI	Tue 9th	10.30 - 10.45	Assessor 2
Aarya	Sharma	Tue 9th	10.30 - 10.45	Assessor 3
Dong	Chen	Tue 9th	10.30 - 10.45	Assessor 4
Lee	Zhung Han	Tue 9th	11.00 - 11.15	Assessor 1
Joe	Seitler	Tue 9th	11.00 - 11.15	Assessor 2
Ziyu	Cui	Tue 9th	11.00 - 11.15	Assessor 3
Ioan	Prince	Tue 9th	11.00 - 11.15	Assessor 4
Lukas	Mykhnenko	Tue 9th	11.15 - 11.30	Assessor 1
Chenghong	Wu	Tue 9th	11.15 - 11.30	Assessor 2
Kirsty	Wei	Tue 9th	11.15 - 11.30	Assessor 3
Muhammad	Abubakar	Tue 9th	11.15 - 11.30	Assessor 4
Wen	Li	Tue 9th	11.30 - 11.45	Assessor 1
Froher	Nabizadah	Tue 9th	11.30 - 11.45	Assessor 2
Harrison	Huang	Tue 9th	11.30 - 11.45	Assessor 3
Patryk	Nowak	Tue 9th	11.30 - 11.45	Assessor 4
Wei	Ooi	Tue 9th	11.45 - 12.00	Assessor 1
Yong Zhi	Tong	Tue 9th	11.45 - 12.00	Assessor 2
Soham	Shah	Tue 9th	11.45 - 12.00	Assessor 3
Yuheng	Fu	Tue 9th	11.45 - 12.00	Assessor 4
Lutfi	Cengiz	Tue 9th	12.00 - 12.15	Assessor 1
Yik	Chan	Tue 9th	12.00 - 12.15	Assessor 2
Run	Zhang	Tue 9th	12.00 - 12.15	Assessor 3
Bavneet	Sehra	Tue 9th	12.00 - 12.15	Assessor 4
Hanna	Semnani	Tue 9th	12.15 - 12.30	Assessor 1
Marios	Avraam	Tue 9th	12.15 - 12.30	Assessor 2
Nicole	Oliveira Costa	Tue 9th	12.15 - 12.30	Assessor 3

Racha	Khedimallah	Wed 10th	09.00 - 09.15	Assessor 1
Simonas	Zalatorius	Wed 10th	09.00 - 09.15	Assessor 2
Thennavan	Kanakarayar	Wed 10th	09.00 - 09.15	Assessor 3
David	Lesman	Wed 10th	09.00 - 09.15	Assessor 4
Rhys	Lloyd	Wed 10th	09.15 - 09.30	Assessor 1
Krish	Thyagarajan	Wed 10th	09.15 - 09.30	Assessor 2
Aaditya	Sharma	Wed 10th	09.15 - 09.30	Assessor 3
Parich	Savetvanich	Wed 10th	09.15 - 09.30	Assessor 4
Junjiang	Wu	Wed 10th	09.30 - 09.45	Assessor 1
Christos	Papazacharias	Wed 10th	09.30 - 09.45	Assessor 2
Krishna	Sookun	Wed 10th	09.30 - 09.45	Assessor 3
Josiah	Tse	Wed 10th	09.30 - 09.45	Assessor 4
Sakthivel	Balaji Perumal	Wed 10th	09.45 - 10.00	Assessor 1
JITONG	CAI	Wed 10th	09.45 - 10.00	Assessor 2
Oluwafunbi	Ogunlaja	Wed 10th	09.45 - 10.00	Assessor 3
Kei	Chan	Wed 10th	09.45 - 10.00	Assessor 4
Roy	Seo	Wed 10th	10.00 - 10.15	Assessor 1
Usayd	Hussain	Wed 10th	10.00 - 10.15	Assessor 2
Chaitanya	Khemani	Wed 10th	10.00 - 10.15	Assessor 3
Sarah	Mahmoud	Wed 10th	10.00 - 10.15	Assessor 4
Ihsaan	Hussain	Wed 10th	10.15 - 10.30	Assessor 1
Hong	Tan	Wed 10th	10.15 - 10.30	Assessor 2
Yee	Lim	Wed 10th	10.15 - 10.30	Assessor 3
Mayan	Maheswaran	Wed 10th	10.15 - 10.30	Assessor 4
Yanzhong	Shi	Wed 10th	10.30 - 10.45	Assessor 1
Charles	Theobald	Wed 10th	10.30 - 10.45	Assessor 2
Adam	Silverwood	Wed 10th	10.30 - 10.45	Assessor 3
Hong	Lim	Wed 10th	10.30 - 10.45	Assessor 4
Marzouk	Hajaij	Wed 10th	11.00 - 11.15	Assessor 1
Kaitlyn	Mistry	Wed 10th	11.00 - 11.15	Assessor 2
Junyuan	Zheng	Wed 10th	11.00 - 11.15	Assessor 3
Summer	Xia	Wed 10th	11.00 - 11.15	Assessor 4
Londrina	Hyseni	Wed 10th	11.15 - 11.30	Assessor 1
Laura	Shaw Barragan	Wed 10th	11.15 - 11.30	Assessor 2
Yi	Tan	Wed 10th	11.15 - 11.30	Assessor 3
Che	SU	Wed 10th	11.15 - 11.30	Assessor 4
Ronak	Kumar	Wed 10th	11.30 - 11.45	Assessor 1
Ensar	Bati	Wed 10th	11.30 - 11.45	Assessor 2
Dominic	De Jonge	Wed 10th	11.30 - 11.45	Assessor 3
Anjum	Jahan	Wed 10th	11.30 - 11.45	Assessor 4
Lexie	Lyu	Wed 10th	11.45 - 12.00	Assessor 1
Chengkun	Yang	Wed 10th	11.45 - 12.00	Assessor 2
Kevin	Song	Wed 10th	11.45 - 12.00	Assessor 3
Claryce	Yap	Wed 10th	11.45 - 12.00	Assessor 4
Long	Yang	Wed 10th	12.00 - 12.15	Assessor 1
Rafael	Langdon	Wed 10th	12.00 - 12.15	Assessor 2
Xin	Ng	Wed 10th	12.00 - 12.15	Assessor 3
Alvaro	Vicente Tarrago	Wed 10th	12.00 - 12.15	Assessor 4
Chun	Ooi	Wed 10th	12.15 - 12.30	Assessor 1
Michael	Wettasinghe	Wed 10th	12.15 - 12.30	Assessor 2
George	Chen	Wed 10th	12.00 - 12.15	Assessor 4