Imperial College London
Department of Electrical & Electronic Engineering

E2 Circuits & Systems – End-of-term Lab Oral 2024

The Final Lab Oral will be in the form of a 15 to 20 minutes oral examination conducted in person in the Lab. This will take place on Wed 11th or Thur 12th of December 2024. The purpose of this end-of-term lab oral is to assess your level of attainment in the intended learning outcomes for Lab 3 to Lab 6, and to give you a chance to "show off" your achievement with the Challenge(s). A schedule for the oral examination is attached. **This is a formal assessment.** If you wish to swap your time slot with someone else, you must find a willing person to swap with, and let me know in advance via email, and no later than Monday 9th of December.

Logbook

You must have your electronics logbook with you at the Oral Examination ready to show to your examiner. Although your logbook will NOT be "marked" in the conventional sense, your examiner will nevertheless judge how much you have engaged and achieved in these second half of the term. You will also be asked questions that can **only** be answered by referring to the logbook.

Challenges

If you managed to complete one or more of the Challenges, you should **take a video** of your achievements and share this with your Assessor. DO NOT PERFORM DEMONSTRATION LIVE. There is not enough time, and it may go wrong on the day.

Format of the Oral – You must arrive in the Level 1 Lab at least 5 minutes before your allocated time. Your Examiner will invite you to join when he/she is ready. You will be asked questions on Lab 3 to Lab 6. These questions are designed to determine how much you understand the principles behind the experiments, how much you have engaged, and how much you have learned. You will also be asked to show demo on any challenges you may have completed.

Grading – Attached is the marksheet that your Examiner will be using during the oral examination. The assessment form with feedback will be returned to you via email. Your will receive a grade for this assessment according to the criteria shown below:

A = Excellent (70%+)	Completed all, and understood everything with no gap in knowledge
B = Good (60%+)	Completed all or nearly all, with good understanding but with minor gaps
C = OK (50%+)	Fair understanding with some gaps, completed most parts
D = Weak (40%+)	Weak understanding with many gaps
E = Fail (below 40%).	Very weak understanding, lack evidence of real effort

We expect the average mark for this assessment to be around 63 to 67% for the entire class. (The average was 66.7% for the mid-term Oral.) To ensure fair assessment, I will perform moderation of marks between different Examiners and apply adjustments as I see fit.

Lab-in-a-Box RETURN

You must return the Lab-in-a-Box AND the DE10-Lite FPGA board to one of the technicians in the Level 1 Lab. They will check the Box's content and record the fact that you have returned the Box. You final Lab Oral marksheet will only be released to you at the start of the term and AFTER you have returned the Box!

Learning Outcomes

Lab 3 & 4 – Counters and Shift Registers

- Explain the workflow in turning a design in SystemVerilog to FPGA bit-stream
- Explain how a basic counter is specified in SystemVerilog
- Explain the link between SystemVerilog and the actual hardware produced (RTL viewer)
- Explain the propagation delay information as reported by Timing Analyzer
- Explain the working of a shift register, LFSR and PRBS
- Explain the concept of using single clock with enable signal
- Explain the binary to BCD conversion algorithm and its use

Lab 5 – DAC and Function Generator

- Explain PWM with LPF as digital to analogue conversion
- Explain limitations and benefits of PWM as a method of DAC
- Explain the working of the DAC chip used in experiment and its specifications
- Explain SPI interface signals
- Explain how to combine counters and other circuits to provide a variable frequency function generator

Lab 6 – ADC and Echo Synthesizer

- Explain the signal flow in the analogue-digital combined system
- Explain why remove of offset to converted digital signal is required
- Explain the "***allpass***" processor module in the context of the basic system
- Explain how the "***single echo***" design works
- Explain how the multiple echo design works

You are expected to complete at least one of the 6 Challenges. The level of difficulty of the Challenges you have completed will also influence the final grade you get.

Peter Cheung
Version 2.4, 3 December 2024.

Imperial College London

Department of Electrical & Electronic Engineering

EE2 Circuits and Systems Module
End-of-term Lab Oral

Name of Student:

Names of Assessors:

Date: Wed/Thur

Performance on the Lab Experiments

1. Logbook Quality and Effectiveness

Highly effective | Effective | OK | Weak | Poor

2. Ability to answer questions from the logbook

Excellent | Good | OK | Poor | Very poor

3. Effort to completing Lab 3 to 6

Fully engaged Strong evidence	Good engagement Good evidence	Acceptable Engagement	Below expected Engagement	V. poor Engagement

4. Challenge attempted or Completed

Challenge completed (say which) | Challenge attempted | Did not attempt

Understanding and Learning Outcomes

5. Understanding of the experiments

Excellent | Good | OK | Poor | Very poor

6. Examiner's opinion on candidate's depth of understanding in general

Broad & deep | Good | Average | Less than average | Poor

FEEDBACK TO STUDENT: **GRADE:**

ELEC50001 Circuits and Systems - End-of-Term Lab Oral Schedule 2024

First name	Surname	Date	Time	Assessor
Ahmad	Jalloh	Wed 11 Dec	9.00 - 9.20	Exam_1
Dan	Rhodes	Wed 11 Dec	9.00 - 9.20	Exam_2
Taj	Choksi	Wed 11 Dec	9.20 - 9.40	Exam_1
Ava	Gifford-Moore	Wed 11 Dec	9.20 - 9.40	Exam_2
Yee	Chee	Wed 11 Dec	9.40 - 10.00	Exam_1
Ahmad	Wahab	Wed 11 Dec	9.40 - 10.00	Exam_2
Ryan	Ong	Wed 11 Dec	9.40 - 10.00	Exam_3
Hyo	Hwang	Wed 11 Dec	9.40 - 10.00	Exam_4
Sam	Mueller-Menrad	Wed 11 Dec	10.00 - 10.20	Exam_1
Tara	Venkatesam	Wed 11 Dec	10.00 - 10.20	Exam_2
Hisham	Khatib	Wed 11 Dec	10.00 - 10.20	Exam_3
Frank	Sun	Wed 11 Dec	10.00 - 10.20	Exam_4
Angeline	Lin	Wed 11 Dec	10.20 - 10.40	Exam_1
Ruizhu	Tian	Wed 11 Dec	10.20 - 10.40	Exam_2
Zhiyuan	Liu	Wed 11 Dec	10.20 - 10.40	Exam_3
Adnan	Ahmed	Wed 11 Dec	10.20 - 10.40	Exam_4
Toby	Clark	Wed 11 Dec	10.40 - 11.00	Exam_1
Kiron	Dutton	Wed 11 Dec	10.40 - 11.00	Exam_2
Chenxuan	Xi	Wed 11 Dec	10.40 - 11.00	Exam_3
Matthew	Dooley	Wed 11 Dec	10.40 - 11.00	Exam_4
Arjun	Vijayanand	Wed 11 Dec	11.00 - 11.20	Exam_1
Louis	Yong	Wed 11 Dec	11.00 - 11.20	Exam_2
Krish	Jindal	Wed 11 Dec	11.00 - 11.20	Exam_3
Neil	Pakrasi	Wed 11 Dec	11.00 - 11.20	Exam_4
Jaime	Rama	Wed 11 Dec	11.20 - 11.40	Exam_1
Dhruba	Fahmiduzzaman	Wed 11 Dec	11.20 - 11.40	Exam_2
Sadig	Sadikhzada	Wed 11 Dec	11.20 - 11.40	Exam_3
Lia	Kommata	Wed 11 Dec	11.20 - 11.40	Exam_4
Edgar	Teh	Wed 11 Dec	11.40 - 12.00	Exam_1
Wei	Xu	Wed 11 Dec	11.40 - 12.00	Exam_2
Nabiha	Saqib	Wed 11 Dec	11.40 - 12.00	Exam_3
Ashis	Gurung	Wed 11 Dec	11.40 - 12.00	Exam_4
Aidan	Mohammed-Ali	Wed 11 Dec	12.00 - 12.20	Exam_1
Mickey	Techachokwiwat	Thu 12 Dec	13.30 - 13.50	Exam_1
Ang	Li	Thu 12 Dec	13.30 - 13.50	Exam_2
Ander	Cobo Puertollano	Thu 12 Dec	13.30 - 13.50	Exam_3
Alex	Brown	Thu 12 Dec	13.30 - 13.50	Exam_4
Maciej	Grzegorczyk	Thu 12 Dec	13.50 - 14.10	Exam_1
Yuki	Hoshino	Thu 12 Dec	13.50 - 14.10	Exam_2
Sam	Hussey	Thu 12 Dec	13.50 - 14.10	Exam_3
Yassine	Serrhini	Thu 12 Dec	13.50 - 14.10	Exam_4
Yael	Miller	Thu 12 Dec	14.10 - 14.30	Exam_1
Jay	Dong	Thu 12 Dec	14.10 - 14.30	Exam_2
Scott	Verdin	Thu 12 Dec	14.10 - 14.30	Exam_3
Rahul	Raghavan	Thu 12 Dec	14.10 - 14.30	Exam_4

Mikhail	Ischenko	Thu 12 Dec	14.30 - 14.50	Exam_1
Benoit	Ben Moubamba	Thu 12 Dec	14.30 - 14.50	Exam_2
Luke	Scully	Thu 12 Dec	14.30 - 14.50	Exam_3
Faris	Kebire	Thu 12 Dec	14.30 - 14.50	Exam_4
Harry	Hill	Thu 12 Dec	14.50 - 15.10	Exam_1
Alfred	Sweet	Thu 12 Dec	14.50 - 15.10	Exam_2
Enid	Maci	Thu 12 Dec	14.50 - 15.10	Exam_3
Jaber	Ahmed	Thu 12 Dec	14.50 - 15.10	Exam_4
Mert	Caka	Thu 12 Dec	15.10 - 15.30	Exam_1
Sami	Marouf	Thu 12 Dec	15.10 - 15.30	Exam_2
Iheanyichukv	Stanley	Thu 12 Dec	15.10 - 15.30	Exam_3
Szymon	Ciba	Thu 12 Dec	15.10 - 15.30	Exam_4
Ali	Rabie	Thu 12 Dec	15.30 - 15.50	Exam_1
Santos	Garcia Valls	Thu 12 Dec	15.30 - 15.50	Exam_2
Lily	Martin	Thu 12 Dec	15.30 - 15.50	Exam_3
Dillon	Jayasinghe	Thu 12 Dec	15.30 - 15.50	Exam_4
Sachin	Sathiyaamoorthy	Thu 12 Dec	15.50 - 16.10	Exam_1
Aditya	Sreekumar	Thu 12 Dec	15.50 - 16.10	Exam_2
Tayo	Babs-Olugbemi	Thu 12 Dec	15.50 - 16.10	Exam_3
Sean	Tam	Thu 12 Dec	15.50 - 16.10	Exam_4
Haris	Mehmood	Thu 12 Dec	16.10 - 16.30	Exam_1