Imperial College London
Department of Electrical & Electronic Engineering

E2 Circuits & Systems – End-of-term Lab Oral 2023

The Final Lab Oral will be in the form of a 15-minutes oral examination conducted in person in the Lab. This will take place between 14-15 December 2022. The purpose of this end-of-term lab oral is to assess your level of attainment in the intended learning outcomes of Lab 3 to Lab 6, and to give you a chance to "show off" your achievement with the Challenge(s). A schedule for the oral examination is attached. **This is a formal assessment.** If you wish to swap your time slot with someone else, you must find a willing person to swap with, and let me know in advance via email, and no later than Monday 12th December.

Logbook

You must have your electronics logbook with you at the Oral Examination ready to show to your examiner. Although your logbook will NOT be "marked" in the conventional sense, your examiner will nevertheless judge how much you have engaged and achieved in these second half of the term. You will also be asked questions that can **only** be answered by referring to the logbook.

Challenges

If you managed to complete one or more of the Challenges, you should **take a video** of your achievements and share this with your Assessor. DO NOT PERFORM DEMONSTRATION LIVE. There is not enough time and it may go wrong on the day.

Format of the Oral – You must arrive in the Level 1 Lab at least 5 minutes before your allocated time. Your Examiner will invite you to join when he is ready. You will be asked questions on Lab 3 to Lab 6. These questions are designed to determine how much you understand the principles behind the experiments, how much you have engaged, and how much you have learned. You will also be asked to show demo on any challenges you may have completed.

Grading – Attached is the marksheet that your Examiner will be using during the oral examination. The assessment form with feedback will be returned to you via email. Your will receive a grade for this assessment according to the criteria shown below:

A = Excellent (70%+)	Completed all, and understood everything with no gap in knowledge
B = Good (60%+)	Completed all or nearly all, with good understanding but with minor gaps
C = OK (50%+)	Fair understanding with some gaps, completed most parts
D = Weak (40%+)	Weak understanding with many gaps
E = Fail (below 40%).	Very weak understanding, lack evidence of real effort

We expect the average mark for this assessment to be around 63 to 67% for the entire class. (The average was 67.3% for the mid-term Oral.) To ensure fair assessment, I will perform moderation of marks between different Examiners and apply adjustments if necessary.

Lab-in-a-Box RETURN

You must return the Lab-in-a-Box to one of the technicians in the Level 1 Lab. They will check the Box's content and record the fact that you have returned the Box. You final Lab Oral marksheet will only be released to you at the start of the term and AFTER you have returned the Box!

Learning Outcomes

Lab 3 & 4 – Counters and Shift Registers

- Explain the workflow in turning a design in SystemVerilog to FPGA bit-stream
- Explain how a basic counter is specified in SystemVerilog
- Explain the link between SystemVerilog and the actual hardware produced (RTL viewer)
- Explain the propagation delay information as reported by Timing Analyzer
- Explain the working of a shift register, LFSR and PRBS
- Explain the concept of using single clock with enable signal
- Explain the binary to BCD conversion algorithm and its use

Lab 5 – DAC and Function Generator

- Explain PWM with LPF as digital to analogue conversion
- Explain limitations and benefits of PWM as a method of DAC
- Explain the working of the DAC chip used in experiment and its specifications
- Explain SPI interface signals
- Explain how to combine counters and other circuits to provide a variable frequency function generator

Lab 6 – ADC and Echo Synthesizer

- Explain the signal flow in the analogue-digital combined system
- Explain why remove of offset to converted digital signal is required
- Explain the "***allpass***" processor module in the context of the basic system
- Explain how the "***single echo***" design works
- Explain how the multiple echo design works

Peter Cheung
Version 2.3, 1 December 2023.

Imperial College London

Department of Electrical & Electronic Engineering

EE2 Circuits and Systems Module
End-of-term Lab Oral

Name of Student:

Names of Assessors:

Date: Wed/Thur

Performance on the Lab Experiments

1. Logbook Quality and Effectiveness

Highly effective | Effective | OK | Weak | Poor

2. Ability to answer questions from the logbook

Excellent | Good | OK | Poor | Very poor

3. Effort to completing Lab 3 to 6

Fully engaged Strong evidence	Good engagement Good evidence	Acceptable Engagement	Below expected Engagement	V. poor Engagement

4. Challenge attempted or Completed

Challenge completed (say which) | Challenge attempted | Did not attempt

Understanding and Learning Outcomes

5. Understanding of the experiments

Excellent | Good | OK | Poor | Very poor

6. Examiner's opinion on candidate's depth of understanding in general

Broad & deep | Good | Average | Less than average | Poor

FEEDBACK TO STUDENT: **GRADE:**

EE2 Circuits and Systems - End-of-term Lab Oral 2023

Surname	First Name	Date	Time	Examiner
Ahmed	Adrib	Wed 13 Dec	10.45 - 11.00	Examiner 3
Ahmed	Ibraheem	Wed 13 Dec	10.00 - 10.15	Examiner 2
Akadiri	Nimi	Wed 13 Dec	09.30 - 09.45	Examiner 2
Akhtar	Rujena	Thur 14 Dec	16.30 - 16.45	Examiner 1
Ang	Ariel En Ren	Thur 14 Dec	15.45 - 16.00	Examiner 1
Aslam	Harun	Thur 14 Dec	16.45 - 17.00	Examiner 1
Banks	Theo	Thur 14 Dec	14.45 - 15.00	Examiner 3
Bhatti	Mehwish Tariq	Wed 13 Dec	09.45 - 10.00	Examiner 3
Bin Khairul Syukri	Arif	Thur 14 Dec	11.15 - 11.30	Examiner 3
Binte Muhamad Nazzim	Aqiilah Nissa	Thur 14 Dec	11.30 - 11.45	Examiner 3
Bishop	Ben	Thur 14 Dec	13.45 - 14.00	Examiner 3
Brown	Theo	Wed 13 Dec	09.00 - 09.15	Examiner 1
Cavan	Cameron	Wed 13 Dec	09.15 - 09.30	Examiner 1
Chachia	Zakariyyaa	Thur 14 Dec	14.15 - 14.30	Examiner 2
Charles	Rolando	Thur 14 Dec	10.15 - 10.30	Examiner 3
Choudhury	Hassan	Thur 14 Dec	13.45 - 14.00	Examiner 1
Costea	Ovidiu	Wed 13 Dec	11.00 - 11.15	Examiner 2
De Vos	Benjamin	Thur 14 Dec	14.45 - 15.00	Examiner 1
Deng	David	Thur 14 Dec	13.30 - 13.45	Examiner 3
Duan	Tom	Wed 13 Dec	10.30 - 10.45	Examiner 2
Edmond Camilus	Dinushan	Thur 14 Dec	10.45 - 11.00	Examiner 3
Ellabban	Ali	Thur 14 Dec	14.30 - 14.45	Examiner 3
Emezie	Jennifer	Wed 13 Dec	12.15 - 12.30	Examiner 1
Falase	Akin	Thur 14 Dec	14.15 - 14.30	Examiner 1
Fernandes	Chris Gabriel	Thur 14 Dec	14.00 - 14.15	Examiner 1
Finka	Abby	Wed 13 Dec	09.15 - 09.30	Examiner 2
Fok	Justin	Wed 13 Dec	11.30 - 11.45	Examiner 1
Giovannetti	Lorenza	Wed 13 Dec	11.00 - 11.15	Examiner 1
Hannibal	Oliver	Thur 14 Dec	13.30 - 13.45	Examiner 1
Hassan	Sophia	Wed 13 Dec	11.30 - 11.45	Examiner 2
Huang	Huang Daniels	Thur 14 Dec	15.15 - 15.30	Examiner 1
Ihebuzor	Chiedozie	Thur 14 Dec	13.30 - 13.45	Examiner 2
Jia	Zhihao	Thur 14 Dec	16.30 - 16.45	Examiner 2
Karapetyan	Alex	Thur 14 Dec	16.15 - 16.30	Examiner 1
Kelly	Maxim Joseph	Thur 14 Dec	15.15 - 15.30	Examiner 2
Khan	Rayyan	Thur 14 Dec	11.00 - 11.15	Examiner 3
Kim	Jinyoung	Wed 13 Dec	12.00 - 12.15	Examiner 1
Kurian	Ajith	Thur 14 Dec	14.15 - 14.30	Examiner 3
Lam	Justin	Wed 13 Dec	10.00 - 10.15	Examiner 3
Landsman	Hannah	Wed 13 Dec	10.15 - 10.30	Examiner 1

Lasanta	Lucas	Thur 14 Dec	14.00 - 14.15	Examiner 3
Li	Quincy	Thur 14 Dec	15.00 - 15.15	Examiner 1
Lin	Zian	Thur 14 Dec	16.15 - 16.30	Examiner 2
Liu	Yuchen	Thur 14 Dec	14.45 - 15.00	Examiner 2
Lo	Anderson KH	Wed 13 Dec	11.45 - 12.00	Examiner 2
Milne	Henry	Wed 13 Dec	10.15 - 10.30	Examiner 3
Misbahul	Intishar Alam	Thur 14 Dec	15.15 - 15.30	Examiner 3
Mohamed	Amin	Thur 14 Dec	15.00 - 15.15	Examiner 3
Moualek	Eddie	Wed 13 Dec	10.15 - 10.30	Examiner 2
Narvaez	Jaime	Thur 14 Dec	15.30 - 15.45	Examiner 2
Ng	Alden	Thur 14 Dec	15.30 - 15.45	Examiner 1
Nkutlwang	Romeo Romeo	Wed 13 Dec	09.30 - 09.45	Examiner 1
Oga	Hector	Thur 14 Dec	16.45 - 17.00	Examiner 2
Olawoye	Adeola	Wed 13 Dec	10.45 - 11.00	Examiner 2
Owens	Isobel	Wed 13 Dec	12.15 - 12.30	Examiner 2
Pasquereau	Arundhathi	Wed 13 Dec	09.30 - 09.45	Examiner 3
Perry	Conrad	Wed 13 Dec	09.00 - 09.15	Examiner 2
Pillai	Charmindhra	Thur 14 Dec	16.00 - 16.15	Examiner 1
Rao	Kiara Kiara	Thur 14 Dec	14.30 - 14.45	Examiner 1
Roche	Alina	Thur 14 Dec	10.00 - 10.15	Examiner 3
Ruda	Dhruv	Wed 13 Dec	09.00 - 09.15	Examiner 3
Ruparelia	Shriya	Wed 13 Dec	0.30 - 10.45	Examiner 3
Sangtani	Varun	Thur 14 Dec	14.30 - 14.45	Examiner 2
Shang	Saxon Zonghan	Wed 13 Dec	10.00 - 10.15	Examiner 1
Shathish	Erin	Thur 14 Dec	15.45 - 16.00	Examiner 2
Shen	Z,C, Charlie	Wed 13 Dec	11.15 - 11.30	Examiner 2
Solanki	Kiertan	Wed 13 Dec	12.00 - 12.15	Examiner 2
Sreekeessoon	Ratnali Shwati	Wed 13 Dec	09.45 - 10.00	Examiner 1
Tan	Samuel MY	Wed 13 Dec	09.45 - 10.00	Examiner 2
Tandon	Veer	Wed 13 Dec	09.15 - 09.30	Examiner 3
Tang	Wenxin	Wed 13 Dec	10.30 - 10.45	Examiner 1
Tetrault	Gabriel	Thur 14 Dec	16.00 - 16.15	Examiner 2
Toussaint	Dylan	Thur 14 Dec	15.00 - 15.15	Examiner 2
Tzartzi	Petroula	Thur 14 Dec	10.30 - 10.45	Examiner 3
Varia	Rishabh	Wed 13 Dec	10.45 - 11.00	Examiner 1
Winters	Dylan Ivor	Wed 13 Dec	11.45 - 12.00	Examiner 1
Xie	Tianchen	Thur 14 Dec	14.00 - 14.15	Examiner 2
Yousif	Rares	Wed 13 Dec	11.15 - 11.30	Examiner 1
Zeng	Tony	Thur 14 Dec	13.45 - 14.00	Examiner 2